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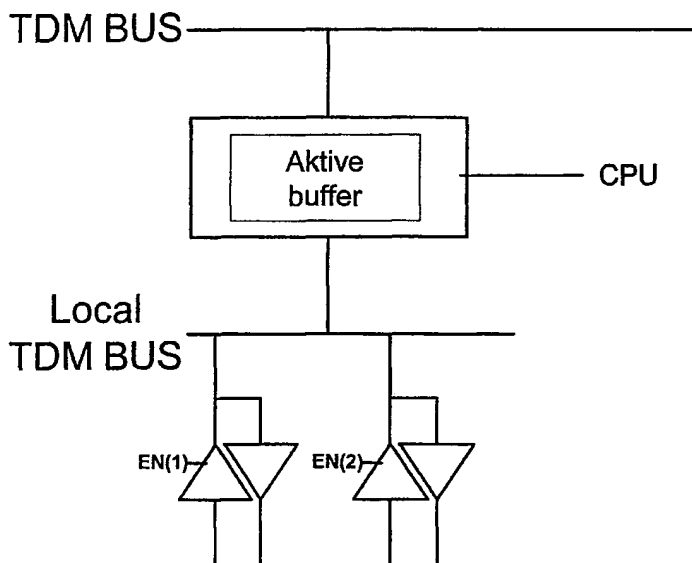
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(54) Title: METHOD FOR REDUCING THE BUS LOAD IN A SYNCHRONOUS DATA BUS SYSTEM



(57) Abstract: The present invention is related to buffering between synchronous circuits communication via a global synchronous bus, and in particular an arrangement for reducing the busload in a TDM bus system by, in a preferred embodiment, introducing a local TEM data bus and an active buffer including a CPU controlled logic between the transceiver loads and the TDM bus. The active buffers in the TX and RX direction together provides a time delay for data travelling from a first local TDM bus out on the backplane TDM bus and back to a second local TDM of the exact duration of one TDM frame or an integer number of TDM frames.



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